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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/783,238	02/20/2004	Keisuke Inoue	SCEI 3.0-187	1362

530 7590 01/16/2008

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ART UNIT	**PAPER NUMBER**
2195	

MAIL DATE	DELIVERY MODE
01/16/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/783,238	INOUE ET AL.	
	Examiner	Art Unit	
	Caroline Arcos	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-55* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-55* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *See Continuation Sheet*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Continuation of Attachment(s) 3). Information Disclosure Statement(s) (PTO/SB/08), Paper No(s)/Mail Date :1/30/2006, 4/24/2006 and 8/24/2006.

DETAILED ACTION

1. Claims 1-55 are pending for examination.

Specification

2. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Double Patenting

3. The non-statutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and In *re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

4. A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

5. Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

6. Claims 10 and 12 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1, 2 and 3 of copending Application No. 09/219,229. Although the conflicting claims are not identical, they are not patentably distinct from each other because both systems comprise substantially the same elements. For example, Claim 10 functions performed by the steps of the instant application are the same and obvious as the steps of claim 1, 2 of copending application No. 09/219,229 (Storing the processor tasks in a shared memory/processor tasks be copied from the shared memory that may be accessed by a plurality of processing units of the multiprocessor computing system/ Plurality of processing units that may access a shared memory, permitting the processing units to determine which of the processor tasks should be executed based on priorities of the processor/ the processing units select processor tasks from shared memory for execution based on priority levels of the processor tasks. The processor tasks that are executed are copied from the shared memory/ providing that the selected processor tasks be copied from the shared memory and executed by one or more of the processing units.)

7. This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented. Double patenting rejection remains until a proper terminal disclaimer is filed.

Claim Rejections - 35 USC § 101

8. 35 U.S.C. 101 reads as follows:

> a. Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

9. Claims 1- 55 are rejected under U.S.C 101 because the claimed invention is directed to non-statutory subject matter.

10. As per claim 1- 55, the claims are non- statutory as they fail to produce a "useful, concrete, and tangible result." *State Street Bank & Trust Co. V. Signature Financial Group Inc. 149 F. 3d 1368, 1373-74 (Fed. Cir. 1998).* The claims are directed to nothing more than an algorithm, failing to indicate how the invention accomplishes a practical application. That is, the claims fall under the judicial exception of an "abstract idea" i.e. an algorithm, which is ineligible for patent protection. Diamond v. Diehr, 450 U.S. 175, 185 (1981).

11. As per claim 29, the claim is non-statutory because it is directed to a method but it is dependent on an apparatus claim, hence it is method and apparatus claim. The claim should be method or apparatus claim, and not both.

Claim Rejections - 35 USC § 112

12. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

13. Claims 1- 55 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

a. The following terms lacks antecedent basis:

(i) The initiating – claim 6.

(ii) the one of the plurality - claim 17.

b. The claim language in the following claims is not clearly understood:

(iii) As per claim 1, , it is not clearly understood the meaning of "processor tasks", are they tasks meant to be executed on a specific processor or are they tasks that are waiting in the queue to be executed or are they tasks that are being executed. Furthermore, it is unclear where "processor tasks" reside.

Line 3, "may access", it is unclear whether or not the processing units access the shared memory. The claim language is broad and indefinite.

Line 5, "selected processor tasks" it is unclear how the selection will be done and what is the criteria. Furthermore, "copied from", it is not clearly understood where it is copied to?

Line 6, " executed by one or more processing units" , it is not clearly understood whether each processor task is executed by only one processor or it can be executed by more than one processing units.

Line 8, it is unclear what is the criteria for "migrating at least one processor task" Does the tasks migrate at all time or is there a condition

for migration. Furthermore, it is not clearly understood the relation between "selected processor tasks" and "processor task".

(iv) As per claim 2, it is unclear whether "prohibiting" shared memory access during the task execution is at all time even if the copied task from the shared memory to the local memory is not a good copy or there is a cache miss.

(v) As per claim 9, line 8, it is not clearly understood if "yielding the first sub-processing unit" is after finishing executing the first processor task or during the execution of the first processing task.

(vi) As per claim 10, it has same deficiency as claim 1. Furthermore, line 13; it is unclear whether "a processor task of higher priority" resides on one of the processing unit or on the shared memory. In addition, line 12, "may be preemptively", it is not clear whether or not the lower priority task running will be preemptively replaced by the higher priority task. The claim language is broad and indefinite.

(vii) As per claim 11, it has same deficiency as claim 2.

(viii) As per claim 14, line 2, it is unclear what is the criteria for "selecting a plurality of processor tasks". Furthermore, line 9, "the plurality of processor tasks" are they tasks that are executing or are they tasks that are waiting for execution in the queue.

(ix) As per claim 17; it is not clearly understood whether initiating the replacement and yielding execution of the processor task is done by the same sub-processing unit or two different sub-processing units.

(x) As per claim 18, it has the same deficiency as claim 17.

(xi) As per claim 21, it is not clearly understood the meaning of "processor tasks", are they tasks meant to be executed on a specific processor or are they tasks that are waiting in the queue to be executed or are they tasks that are being executed. line,9, it is unclear whether "prohibiting" shared memory access during the task execution is at all time even if the copied task from the shared memory to the local memory is not a good copy or there is a cache miss. Line 11, "selecting a plurality of processor tasks" it is unclear how the selection will be done and what is the criteria.

(xii) As per claim 21, line3, "may be preemptively", it is not clearly understood whether or not the lower priority task will be preemptively replaced. The claim language is indefinite. Furthermore, line 4, it is not clear what is the relation between "a processor task of higher priority" and "the n-th processor task" of line 15 in claim 21.it is not clear whether it is the same processor task or different task.

(xiii) As per claim 24, line 2, it is not clearly understood what is meant by "entries of for sub-processing unit identifiers". Does the priority table have all sub-processing units ID available or specific sub- processing ID

that is needed to execute each task? Line 6, it is unclear what is meant by "identifier pair". Furthermore, line 7, it is not clearly understood if the shared task priority included processor task is currently running or scheduled to run (waiting).

(xiv) As per claim 25, line 4, it is not clear who "searches the shared task". Line 5, it is not clearly understood what is meant by "entry pair". Furthermore, it is not clearly understood how determining higher priority task will be achieved by indicating lower priority task. It is not clear if the sub-processing unit is determining highest priority or higher priority.

(xv) As per claim 26, it has the same deficiency as claim 21.

(xvi) As per claim 27, it has the same deficiency as claim 1. Furthermore, line 10, it is unclear whether "processor task is migrated" at all time or what are the criterias for migration of processor task from one processing units to another.

(xvii) As per claim 28, it has the same deficiency as claim 2.

(xviii) As per claim 35, it has the same deficiency as claim 9.

(xix) As per claim 36, line 5, it is unclear where "an n-th processor task" reside. Is it on one of the plurality of processing unit or is it in the shared memory waiting to be executed. Furthermore, line 8, it is not clearly understood whether "the plurality of processor tasks" are running/executing tasks or waiting to be executed tasks.

(xx) As per claim 39, it is unclear whether the sub-processing unit initiating the replacement and the one performing the yielding is the same processing units or different processing units.

(xxi) As per claim 43, it has same deficiency as claim 1.

(xxii) As per claim 45, line 6, it is not clearly understood what is meant by "on the of sub-processing units".

(xxiii) As per claim 50, line 3, it is not clearly understood whether "lower priority" is the same as "lowest priority" of line 4 in claim 48.

(xxiv) As per claim 53, it has the same deficiency as claim 24.

Claim Rejections - 35 USC § 102

14. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

15. Claims 10 and 12-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Bahr (EP 0459931 A2).

16. As per claim 10, Bahr teaches a method of executing processor tasks on a multi-processing system, the multi-processing system including a plurality of processing units that may access a shared memory(abs. Lines 1-3), the method comprising:

providing that selected processor tasks be copied from the shared memory and executed by one or more of the processing units(Col.6, lines 27-31);

providing that the processing units select processor tasks from the shared memory for execution based on priority levels of the processor tasks(col.1, lines 12-14; col.1, lines 28-30); and

providing that a processor task of lower priority running on one of the processing units may be preemptively replaced with a processor task of higher priority(col.1, lines 22-28).

17. As per claim 12, Bahr teaches that the plurality of processing units comprises a main processor unit and a plurality of sub-processing units, each of the plurality of sub-processing units having a local memory(abs, lines 1-3), and wherein the processor tasks are copied to local memory(col.6, lines 40-42) and executed in local memory(col.6, lines 50-53).

18. As per claim 13, Bahr teaches that the requirement that the sub-processing units select a processor task of higher priority before a processor task of lower priority from the shared memory(Col. 7, lines 23-26; col. 8, lines 15-16); col. 9, lines 29-30).

19. As per claim 14, Bahr teaches selecting a plurality of processor tasks of associated priority levels from the shared memory for execution by a number of sub-processing units (col.7, lines 23-27);

causing an n-th processor task in the shared memory having a given priority level to become ready for execution; and

determining whether the given priority level is higher than any of the priority levels of the plurality of processor tasks (col.1, lines 22-25).

20. As per claim 15, Bahr teaches that at least one of the sub-processing units is operable to perform the determination (col.1, lines 22-25).

21. As per claim 16, Bahr teaches preemptively replacing one of the plurality of processor tasks of lower priority level than the given priority level with the n-th processor task (col.1, lines 22-28).

Claim Rejections - 35 USC § 103

22. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

23. Claims 1- 4, 8-9, 27-30, 34-38 and 41-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bahr et al. (EP-0459931 A2), in view of Abramson et al. (Abramson) (Us 5,506,987).

24. Bahr et al. (EP-0459931 A2) is introduced in the IDS presented by the applicant

25. As per claim 1, Bahr teach the invention substantially as claimed including a method of executing processor tasks on a multi-processing system, the multi-processing system including a plurality of processing units that may access a shared memory (abs. Lines 1-3), the method comprising:

providing that selected processor tasks be copied from the shared memory and executed by one or more of the processing units(Col.6, lines 27-31).

26. Bahr did not specifically teach migrating at least one processor task from one of the processing units to another of the processing units. However, Abramson teaches migrating at least one processor task from one of the processing units to another of the processing units (abs, lines 25-29; col. 4, lines 22-26).

27. It would have been obvious to one of an ordinary skill in the art at the time the invention was made to have combined the teaching of Bahr and Abramson because Abramson's teaching of migrating the task from one processing unit to another would improve the balance of the system workload.

28. As per claim 2, Bahr did not explicitly teach prohibiting the execution of the processor task from the shared memory (Col.6, lines 40-45; col.6, lines 50-53). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to prohibit the

execution of the task from the shared memory to eliminate unnecessary memory access since the task is copied to the local memory. Therefore, one would be motivated to utilize this concept to improve the overall memory access efficiency.

29. As per claim 3, Bahr teaches wherein the plurality of processing units comprises a main processor unit and a plurality of sub-processing units, each of the plurality of sub-processing units having a local memory(abs, lines 1-3) and wherein the processor tasks are copied to local memory(col.6, lines 40-42) and executed in local memory(col.6, lines 50-53).

30. As per claim 4, Abramson teaches that the migration of the at least one processor task is based on a condition (abs, lines 24-29; col.7, lines 7-10).

31. As per claim 8, Bahr teaches the requirement that the sub-processing units select a processor task of higher priority before a processor task of lower priority from the shared memory(Col. 7, lines 23-26; col. 8, lines 15-16); col. 9, lines 29-30).

32. As per claim 9, Bahr teaches selecting a first processor task of a first priority level from the shared memory for execution by a first sub-processing unit;

selecting a second processor task of a second priority level from the shared memory for execution by a second sub-processing unit(col.3, lines 14-27;col. 9, lines 29-30) ; and

yielding the first sub-processing unit to a third processor task of a third priority level, the third processor task being selected because its priority level is higher than any other

processor tasks that a ready to be executed (col.1, lines 26-28).

33. As per claim 27, Bahr teaches a multi-processor apparatus, comprising:

a plurality of processing units, each processing unit including local memory in which to execute processor tasks (abs, 1-3; col. 6, lines 50-53); and

a shared memory operable to store processor tasks that are ready to be executed, wherein:

the processor tasks are copied from the shared memory into the local memory of the processing units to execute them (col.6, lines 40-45).Bahr did not teach that at least one processor task is migrated from one of the processing units to another of the processing units. However, Abramson teaches that at least one processor task is migrated from one of the processing units to another of the processing units (abs, lines 25-29).

35. As per claim 28, Bahr did not explicitly teach prohibiting the execution of the processor task from the shared memory (Col.6, lines 40-45; col.6, lines 50-53). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to prohibit the execution of the task from the shared memory to eliminate unnecessary memory access since the task is copied to the local memory. Therefore, one would be motivated to utilize this concept to improve the overall memory access efficiency.

36. As per claim 29, Bahr teaches the plurality of processing units comprises a main processor unit and a plurality of sub-processing units, each of the plurality of sub-processing units having a local memory (abs, lines1-3), and wherein the processor tasks are copies to local

memory and executed in local memory(col.6, lines 40-46).

37. As per claim 30, it is the apparatus claim of the method claim 4. Therefore, it is rejected for the same rational as claim 4.

38. As per claim 34, Bahr teaches that the sub-processing units are operable to select a processor task of higher priority before a processor task of lower priority from the shared memory (col. 7, lines 23-27).

39. As per claim 35, it is the apparatus claim of claim 9. Therefore, it is rejected for the same reason as claim 9.

40. As per claim 36, Bahr teaches that the sub-processing units are operable to:

select a plurality of processor tasks of associated priority levels from the shared memory for execution (col. 7, lines 23-27); and

determine whether an n-th processor task in the shared memory having a given priority level that has become ready for execution has a higher level priority than any of the priority levels of the plurality of processor tasks (col.1, lines 24-28).

41. As per claim 37, Bahr teaches that at least one of the sub-processing units is operable to perform the determination (col.1, lines 24-28).

42. As per claim 38, Bahr teaches that at least one of the sub-processing units is operable to preemptively replace one of the plurality of processor tasks of lower priority level than the given priority level with the n-th processor task (col.1, lines 24-28).

43. As per claim 41, Bahr teaches that the yielding sub-processing unit is operable to write the processor task of lower priority from its local memory back into the shared memory (col.1, lines 26-28; col.6, lines 31-33).

44. As per claim 42, Bahr teach the yielding sub-processing unit is operable to copy the n-th processor task of higher priority from the shared memory into its local memory for execution (col.1, lines 22-28; col.7, lines 23-27).

45. Claim 11 and 21-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bahr et al. (EP-0459931 A2).

46. As per claim 11, Bahr did not explicitly teach prohibiting the execution of the processor task from the shared memory (Col.6, lines 40-45; col.6, lines 50-53). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to prohibit the execution of the task from the shared memory to eliminate unnecessary memory access since the task is copied to the local memory. Therefore, one would be motivated to utilize this concept to improve the overall memory access efficiency.

47. As per claim 21, Bahr teaches a method of executing processor tasks on a multi-processing system, the multi-processing system including a plurality of sub-processing units and a main processing unit that may access a shared memory(abs. Lines 1-3), each sub-processing unit including an on-chip local memory separate from the shared memory(col.1, lines 49-51), the method comprising:

providing that the processor tasks be copied from the shared memory into the local memory of the sub-processing units in order to execute them(Col.6, lines 27-31), and

selecting a plurality of processor tasks of associated priority levels from the shared memory for execution by a number of sub-processing units(Col.7, lines 23-27);

providing that the sub-processing units may determine whether an n-th processor task in the shared memory having a given priority level is higher than any of the priority levels of the plurality of processor tasks(col.1, lines 22-28).

48. Bahr did not explicitly teach prohibiting the execution of the processor task from the shared memory (Col.6, lines 40-45; col.6, lines 50-53). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to prohibit the execution of the task from the shared memory to eliminate unnecessary memory access since the task is copied to the local memory. Therefore, one would be motivated to utilize this concept to improve the overall memory access efficiency.

49. As per claim 22, Bahr teaches that a processor task of lower priority running on one of the sub-processing units may be preemptively replaced with a processor task of higher priority

(col.1, lines 22-28).

50. As per claim 23, Bahr teaches that the sub-processing units use a shared task priority table in determining whether the n-th processor task is of a higher priority level than the plurality of processor tasks (Col.1, lines 19-25).

51. As per claim 24, Bahr teaches that the shared task priority table includes entries of for sub-processing unit identifiers and processor task priority identifiers; and

each entry includes a sub-processing unit identifier and priority identifier pair that indicate a priority level of a given processor task running on an associated sub-processing unit (col.7, lines 23-26; col.7, lines 32-43).

52. As per claim 25, Bahr teaches that providing that a sub-processing unit seeking to determine whether the n-th processor task is of a higher priority level than the plurality of processor tasks searches the shared task priority table to find an entry pair indicating a lower priority level (col.1, lines 22-26; col.3, lines 14-16; col. 7, lines 25-26).

53. Claims 17-20, 26, 43-50 and 53-55 are rejected under 35 U.S.C. 103(a) as being anticipated by Bahr et al. (EP-0459931 A2), in view of Gaetner (US 5,452,452).

54. As per claim 17, Bahr did not explicitly teach that one or more of the sub-processing units is operable to at least initiate the replacement and cause the one of the plurality of sub-

processing units to yield execution of the processor task of lower priority level (col.1, lines 26-28).

55. However, Gaetner teaches that one or more of the sub-processing units is operable to at least initiate the replacement and cause the one of the plurality of sub-processing units to yield execution of the processor task of lower priority level (col.6, lines 64-67; col.8, lines 1-5).

56. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Bahr and Gaetner because Gaetner's teaching of migrating tasks based on their priority level would improve the overall system efficiency by executing tasks that require immediate attention.

57. As claim 18, Gaetner teaches that the initiating sub-processing unit issues an interrupt to the yielding sub-processing unit in order to initiate the replacement of the processor task of lower priority level.

58. As per claim 19, Bahr teaches that providing that the yielding sub-processing unit writes the processor task of lower priority from its local memory back into the shared memory (col.6, lines 31-33).

59. As per claim 20, Bahr teaches that providing that the yielding sub-processing unit copies the n-th processor task of higher priority from the shared memory into its local memory for

execution (col.1, lines 24-28; col.7, lines 23-26).

60. As per claim 26, Bahr teaches a method of executing processor tasks on a multi-processing system, the multi-processing system including a plurality of sub-processing units and a main processing unit that may access a shared memory , each processing unit including an on-chip local memory separate from the shared memory(abs, lines 1-3), the method comprising:

providing that the processor tasks be copied from the shared memory into the local memory of the sub-processing units in order to execute them(Col.6, lines 27-31);

providing that the sub-processing units select processor tasks from the shared memory for execution based on priority levels of the processor tasks(Col.7, lines 23-27).

61. Bahr did not explicitly teach prohibiting the execution of the processor task from the shared memory (Col.6, lines 40-45; col.6, lines 50-53) and migrating a processor task of higher priority running on a given one of the sub-processing units to another of the sub-processing units running a processor task of lower priority in response to an interrupt received by the given sub-processing unit.

62. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to prohibit the execution of the task from the shared memory to eliminate unnecessary memory access since the task is copied to the local memory. Therefore, one would be motivated to utilize this concept to improve the overall memory access efficiency.

63. However, Gaetner teaches migrating a processor task of higher priority running on a given one of the sub-processing units to another of the sub-processing units running a processor

task of lower priority in response to an interrupt received by the given sub-processing unit (col.7, lines 56-58; col. 8, lines 1-5).

64. As per claim 43, Bahr teaches a multi-processor apparatus, comprising:

a plurality of sub-processing units, each sub-processing unit including an on-chip local memory in which to execute processor tasks (abs., lines 1-2); and

a shared memory operable to store processor tasks that are ready to be executed (abs., lines 2-3; col. 7, lines 23-27), wherein:

the processor tasks are copied from the shared memory into the local memory of the sub-processing units in order to execute them(col.6, lines 35-43), and that the processor tasks are not executed from the shared memory (Col.6, lines 35-42),

the sub-processing units are operable to select processor tasks from the shared memory for execution based on priority levels of the processor tasks (col.7, lines 25-27; col.8, lines 14-16; col9, lines 29-30).

65. Bahr did not teach that at least one of the sub-processing units is operable to migrate a processor task of higher priority running on a given one of the sub-processing units to another of the sub-processing units running a processor task of lower priority in response to an interrupt received by the given sub-processing unit.

66. However, Gaetner teaches that at least one of the sub-processing units is operable to migrate a processor task of higher priority running on a given one of the sub-processing units to

another of the sub-processing units running a processor task of lower priority in response to an interrupt received by the given sub-processing unit (col.8, lines 1-5).

67. As per claim 44, Bahr teaches that the sub-processing units are operable to select a processor task of higher priority before a processor task of lower priority from the shared memory (col.9, lines 29-30).

68. As per claim 45, Bahr teaches that the sub-processing units are operable to:

select a plurality of processor tasks of associated priority levels from the shared memory for execution (col. 1, lines 22-30; col.23, lines 14-17).

69. Bahr did not teach explicitly to determine which of the plurality of processor tasks running on the of sub-processing units has a lowest priority level that is lower than the priority level of the processor task running on the given sub-processing unit. However, Gaetner teaches that determine which of the plurality of processor tasks running on the of sub-processing units has a lowest priority level that is lower than the priority level of the processor task running on the given sub-processing unit (col. 8, lines 3-7).

70. As per claim 46, Bahr teaches that the given sub-processing unit is operable to perform the determination (col. 1, lines 22-30).

71. As per claim 47, Gaetner teaches that the given processor task is migrated to the sub-processing unit running the processor task of lowest priority level and replacing the lowest priority processor task (col.7, lines 31-34; col.8, lines 3-5).

72. As per claim 48, Gaetner teaches that the given sub-processing unit is operable to at least initiate the migration and causing the sub-processing unit running the processor task of lowest priority level to yield execution to the given processor task of higher priority level(col.6, lines 64-69; col. 8, lines 1-5).

73. As per claim 49, Gaetner teaches that the given sub-processing unit is operable to issue an interrupt to the yielding sub-processing unit in order to initiate the replacement of the processor task of lowest priority level(col.8, lines 1-5).

74. As per claim 50, Bahr teaches that the yielding sub-processing unit is operable to write the processor task of lower priority from its local memory back into the shared memory (col.1, lines 24-28).

75. As per claim 52, Bahr teaches that the given sub-processing unit is operable to use a shared task priority table in determining which processor task is of the lowest priority level (col.3, lines 14-16; col. 7, lines 25-26).

76. As per claim 53, it is the apparatus claim of the method claim 24. Therefore, it is rejected under the same rational as claim 24.

77. As per claim 54, Bahr teaches that the given sub-processing unit is operable to search the shared task priority table to find an entry pair indicating a lowest priority level (col.3, lines 14-16; col. 7, lines 25-26).

78. As per claim 55, Gaetner teaches that the sub-processing units are operable to modify the shared task priority table such that the entry pairs are current (col.4, lines 6-13; col. 5, lines 23-25).

79. Claims 5-7, 31-33, 39-40 and 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bahr et al. (EP-0459931 A2), in view of Abramson (US 5,506,987) and further in view of Gaetner et al. (Gaetner) (US 5,452,452) .

80. Gaetner et al. (Gaetner) (US 5,452,452) was introduced in the IDS.

81. As per claim 5, the combined method of Bahr and Abramson did not teach that the condition is based on respective priority levels associated with the processor tasks. However, Gaetner teaches that the condition is based on respective priority levels associated with the processor tasks (col.7, lines 56-58).

82. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Bahr, Abramson and Gaetner because Gaetner's teaching of migrating tasks based on their priority level would improve the overall system efficiency by executing tasks that require immediate attention.

83. As per claim 6, Abramson teaches that the satisfaction of the condition and the initiating of the migration is not based on preemptive action (col.9, lines 28-34).

84. As per claim 7, Bahr teaches the invention including requiring that the sub-processing units select processor tasks from the shared memory for execution based on their priority levels (col.1, lines 12-14; col.1, lines 28-30).

85. As per claim 31, Gaetner teaches that the condition is based on respective priority levels associated with the processor tasks (col.8, lines 3-5).

86. As per claim 32, it is the apparatus claim of the method claim 6. Therefore, it is rejected for the same rational as claim 6.

87. As per claim 33, Bahr teaches that the sub-processing units are operable to select processor tasks from the shared memory for execution based on their priority levels (col.1, lines 19-28; col.3, lines 14-16).

88. As per claim 39, it is the apparatus claim of the method claim 17. Therefore, it is rejected under the same rational as claim 17.

89. As per claim 40, Gaetner teaches that the initiating sub-processing unit is operable to issue an interrupt to the yielding sub-processing unit in order to initiate the replacement of the processor task of lower priority level (col. 6, lines 64-67; col.col.8, lines 1-5).

90. As per claim 51, Abramson teaches that the yielding sub-processing unit is operable to copy the given processor task of higher priority from the local memory of the given sub-processing unit into its local memory for execution (col.1, lines 60-64).

Conclusion

91. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

(US 2002/002578) Teaches migration of a job from one PE to another.

(US 5,630,128) teaches lower priority process yield to the higher priority process.

92. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Caroline Arcos whose telephone number is 571-270-3151. The examiner can normally be reached on Monday-Thursday 7:00 AM to 5:30 PM.

93. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on 571-272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

94. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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